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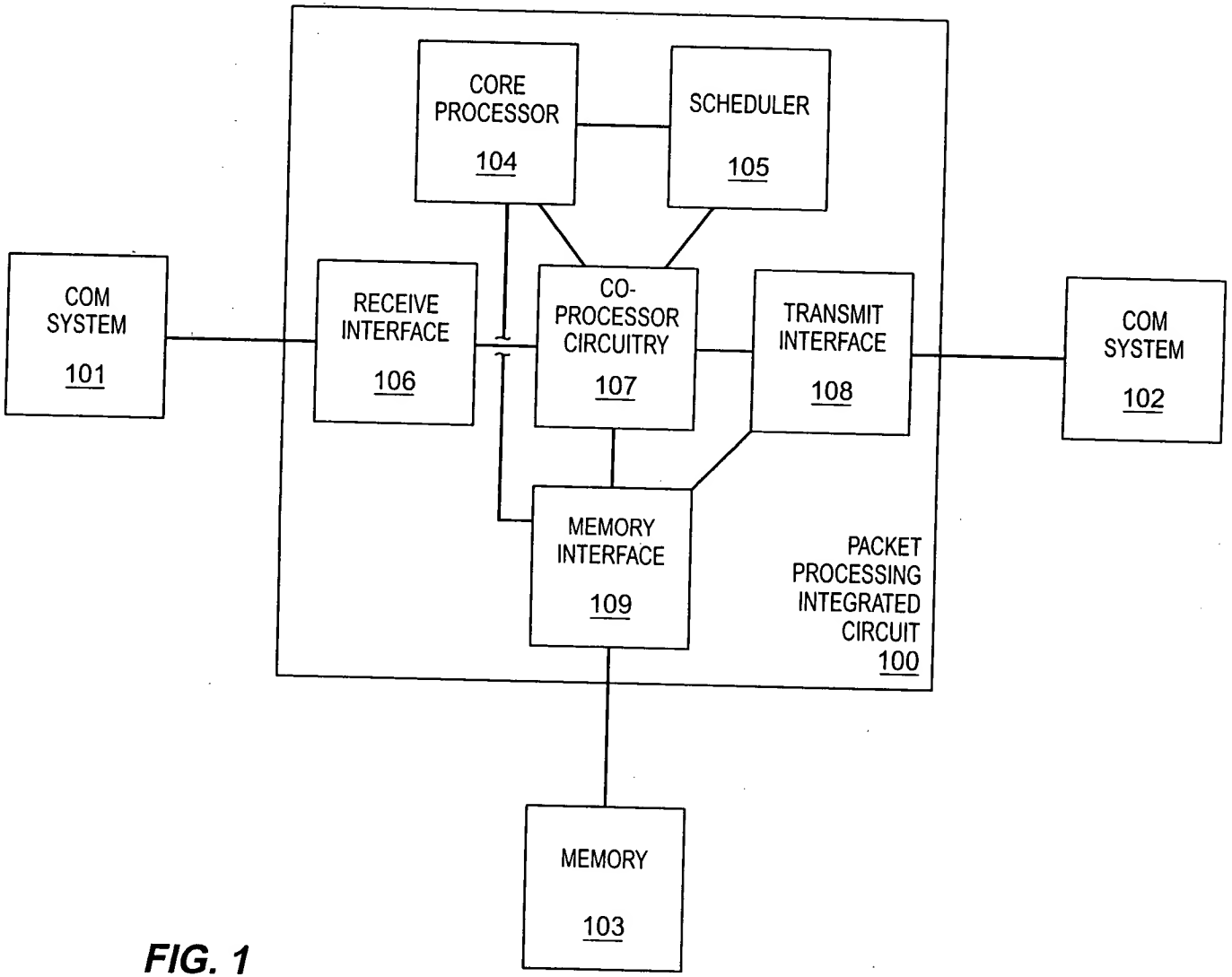


FIG. 1

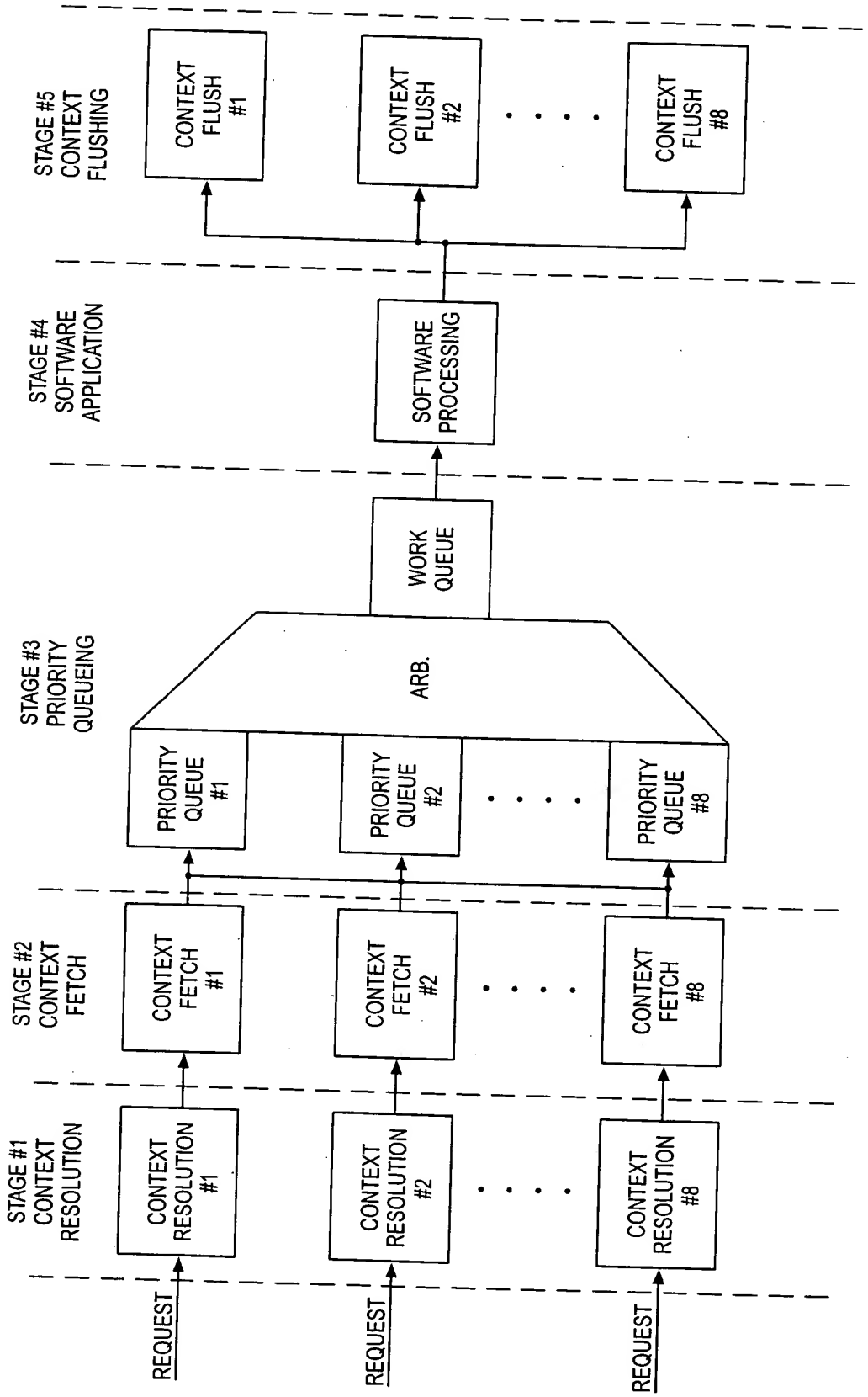

STAGE #1 CONTEXT RESOLUTION
STAGE #2 CONTEXT FETCH
STAGE #3 PRIORITY QUEUEING
STAGE #4 SOFTWARE APPLICATION
STAGE #5 CONTEXT FLUSHING
REQUEST
REQUEST
REQUEST
CONTEXT RESOLUTION #1
CONTEXT RESOLUTION #2
CONTEXT RESOLUTION #8
CONTEXT FETCH #1
CONTEXT FETCH #2
CONTEXT FETCH #8
PRIORITY QUEUE #1
PRIORITY QUEUE #2
PRIORITY QUEUE #8
ARB.
WORK QUEUE
SOFTWARE PROCESSING
CONTEXT FLUSH #1
CONTEXT FLUSH #2
CONTEXT FLUSH #8

FIG. 2

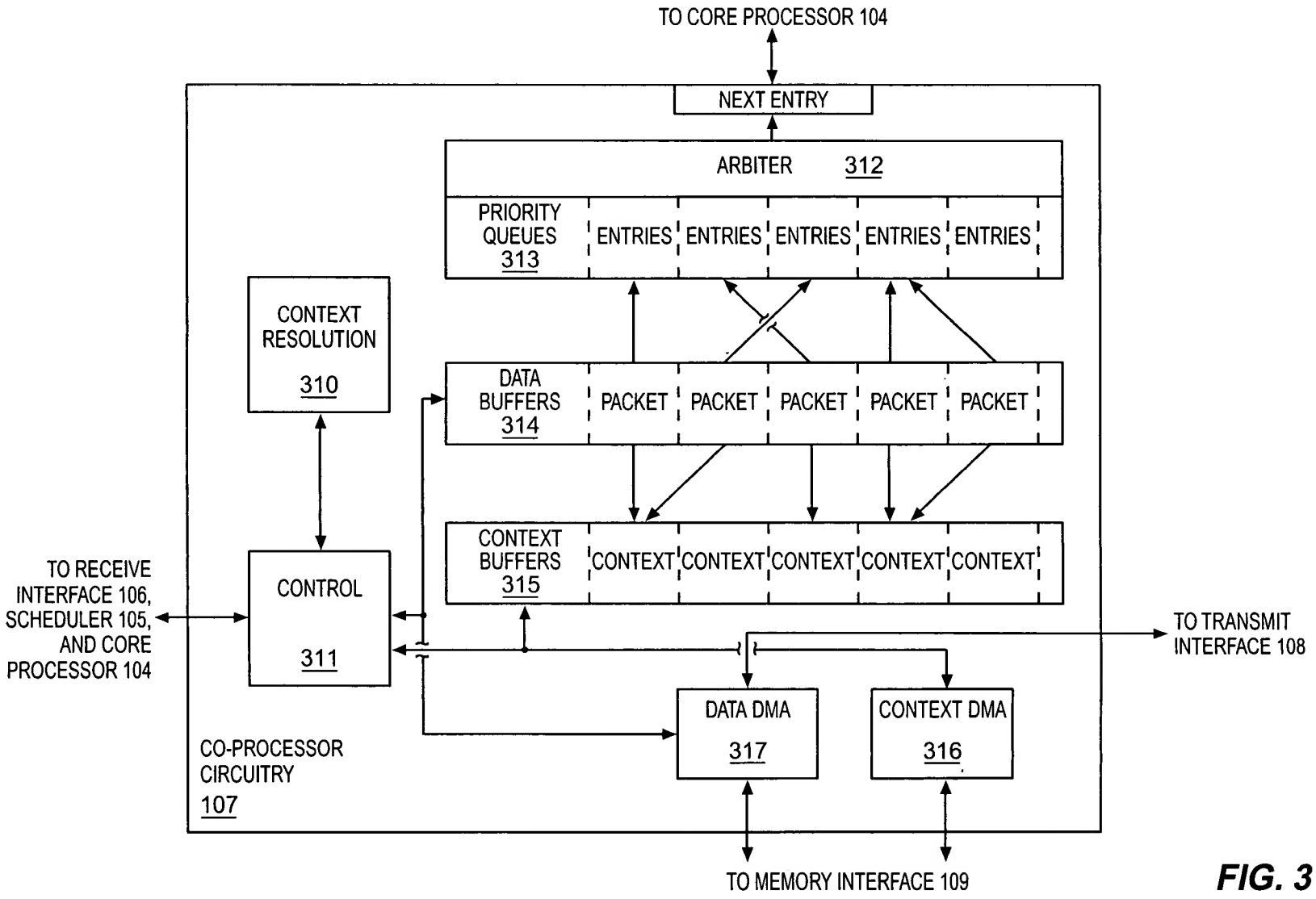
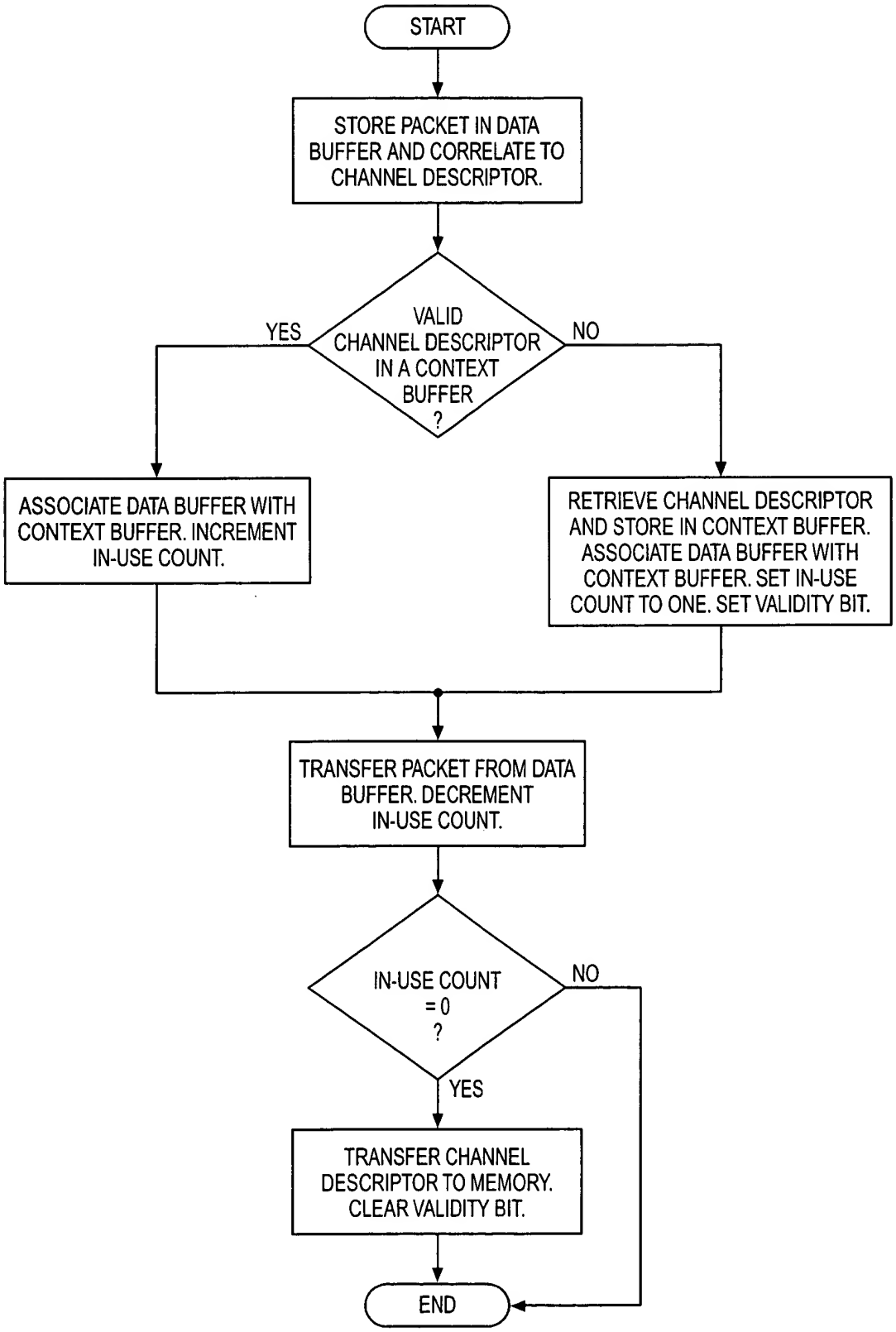

TO CORE PROCESSOR 104
NEXT ENTRY
ARBITER 312
PRIORITY QUEUES 313
ENTRIES
ENTRIES
ENTRIES
ENTRIES
ENTRIES
CONTEXT RESOLUTION 310
DATA BUFFERS 314
PACKET
PACKET
PACKET
PACKET
PACKET
CONTEXT BUFFERS 315
CONTEXT
CONTEXT
CONTEXT
CONTEXT
CONTEXT
TO RECEIVE INTERFACE 106, SCHEDULER 105, AND CORE PROCESSOR 104
CONTROL 311
TO TRANSMIT INTERFACE 108
DATA DMA 317
CONTEXT DMA 316
CO-PROCESSOR CIRCUITRY 107
TO MEMORY INTERFACE 109

FIG. 3

FIG. 4


START
STORE PACKET IN DATA BUFFER AND CORRELATE TO CHANNEL DESCRIPTOR.
VALID CHANNEL DESCRIPTOR IN A CONTEXT BUFFER ?
YES
NO
ASSOCIATE DATA BUFFER WITH CONTEXT BUFFER. INCREMENT IN-USE COUNT.
RETRIEVE CHANNEL DESCRIPTOR AND STORE IN CONTEXT BUFFER. ASSOCIATE DATA BUFFER WITH CONTEXT BUFFER. SET IN-USE COUNT TO ONE. SET VALIDITY BIT.
TRANSFER PACKET FROM DATA BUFFER. DECREMENT IN-USE COUNT.
IN-USE COUNT = 0 ?
NO
YES
TRANSFER CHANNEL DESCRIPTOR TO MEMORY. CLEAR VALIDITY BIT.
END

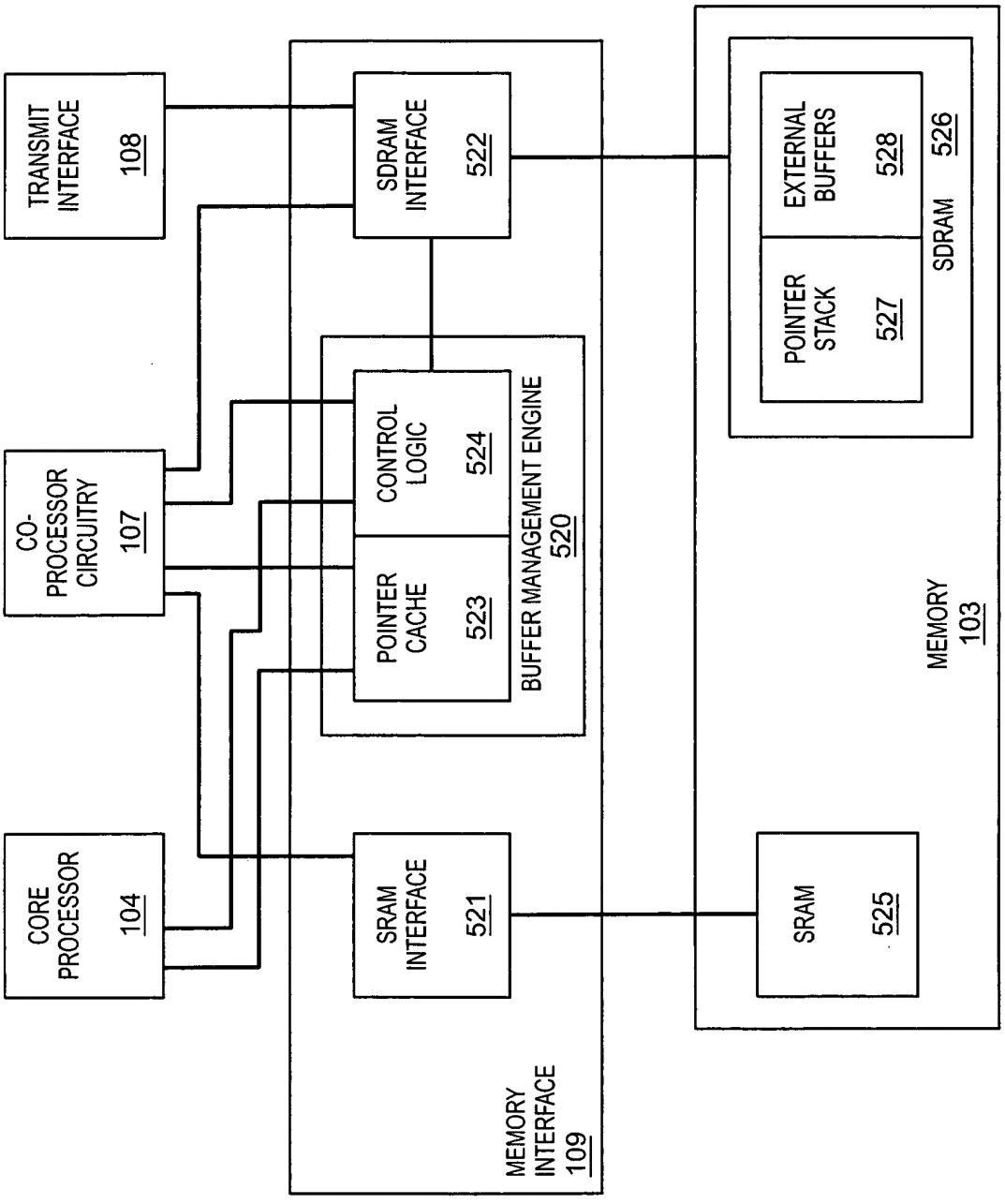

TRANSMIT INTERFACE 108
CO-PROCESSOR CIRCUITRY 107
CORE PROCESSOR 104
SDRAM INTERFACE 522
CONTROL LOGIC 524
POINTER CACHE 523
BUFFER MANAGEMENT ENGINE 520
SRAM INTERFACE 521
MEMORY INTERFACE 109
POINTER STACK 527
EXTERNAL BUFFERS 528
SDRAM 526
SRAM 525
MEMORY 103

FIG. 5

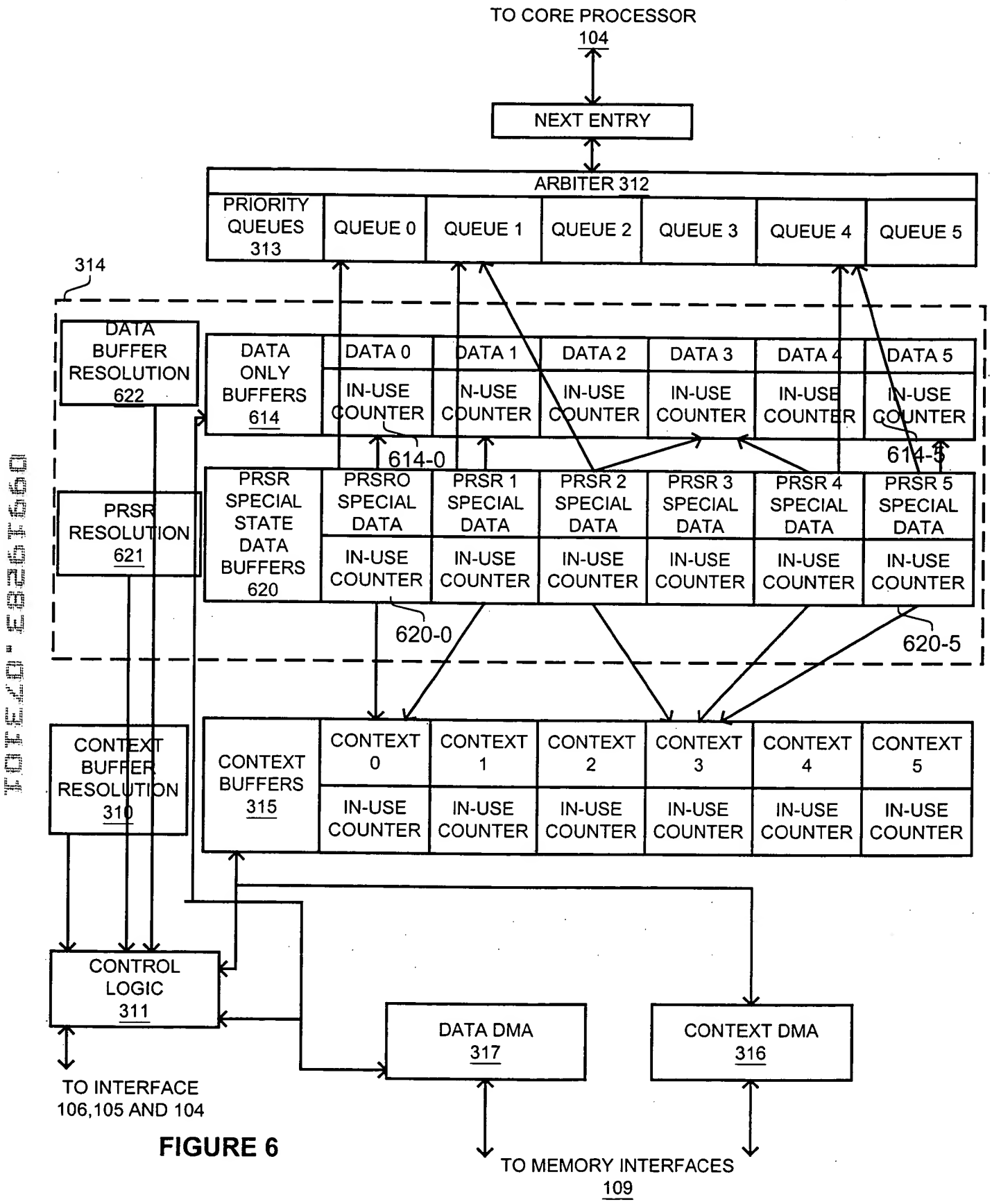

TO CORE PROCESSOR
104
NEXT ENTRY
ARBITER 312
PRIORITY QUEUES 313
QUEUE 0
QUEUE 1
QUEUE 2
QUEUE 3
QUEUE 4
QUEUE 5
314
DATA BUFFER RESOLUTION 622
DATA ONLY BUFFERS 614
DATA 0
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
IN-USE COUNTER
614-0
614-5
PRSR RESOLUTION 621
PRSR SPECIAL STATE DATA BUFFERS 620
PRSRO SPECIAL DATA
PRSR 1 SPECIAL DATA
PRSR 2 SPECIAL DATA
PRSR 3 SPECIAL DATA
PRSR 4 SPECIAL DATA
PRSR 5 SPECIAL DATA
620-0
620-5
CONTEXT BUFFER RESOLUTION 310
CONTEXT BUFFERS 315
CONTEXT 0
CONTEXT 1
CONTEXT 2
CONTEXT 3
CONTEXT 4
CONTEXT 5
CONTROL LOGIC 311
DATA DMA 317
CONTEXT DMA 316
TO INTERFACE 106,105 AND 104
TO MEMORY INTERFACES 109

FIGURE 6

EP 1 276 289 A2

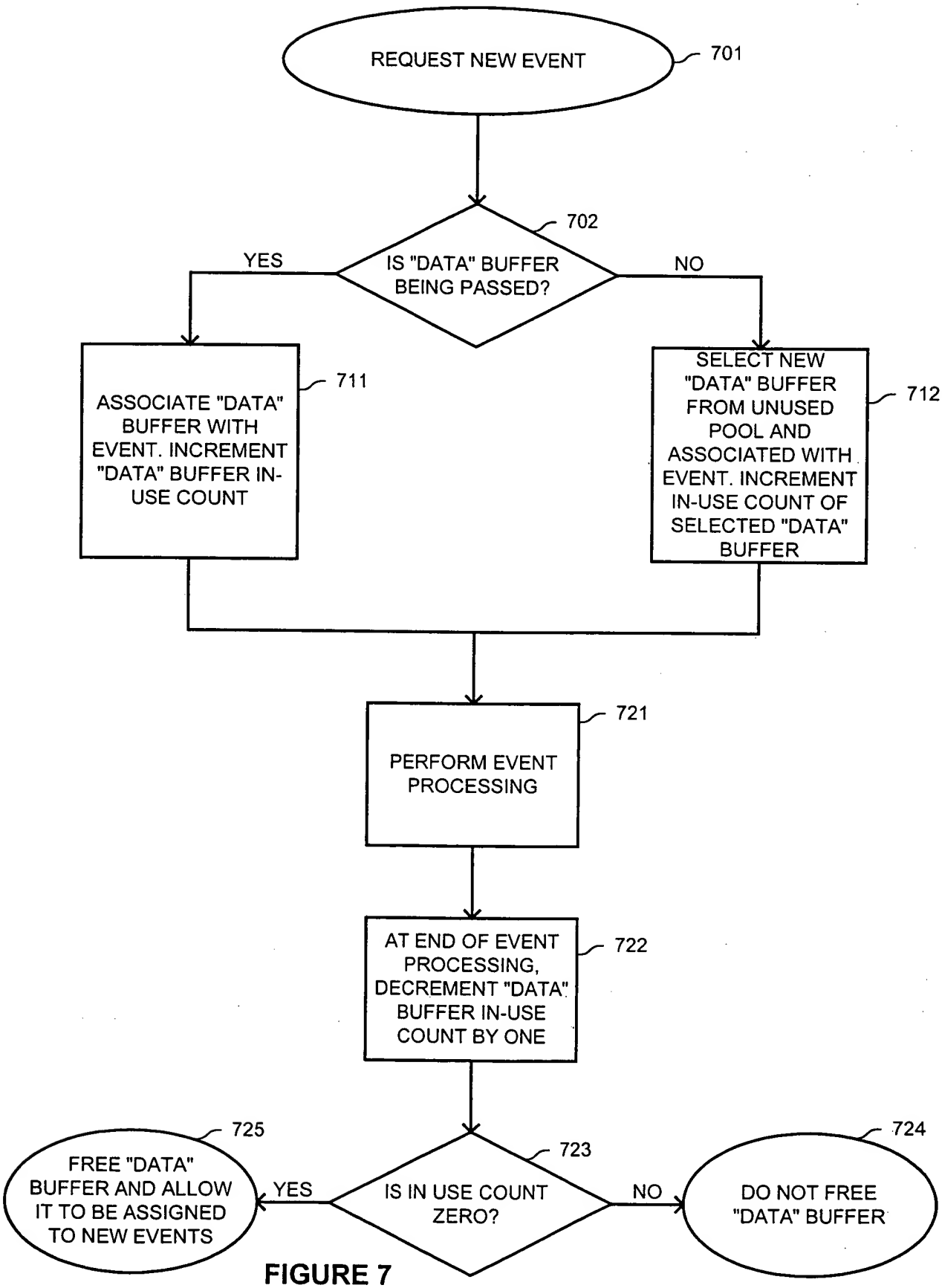


FIGURE 7

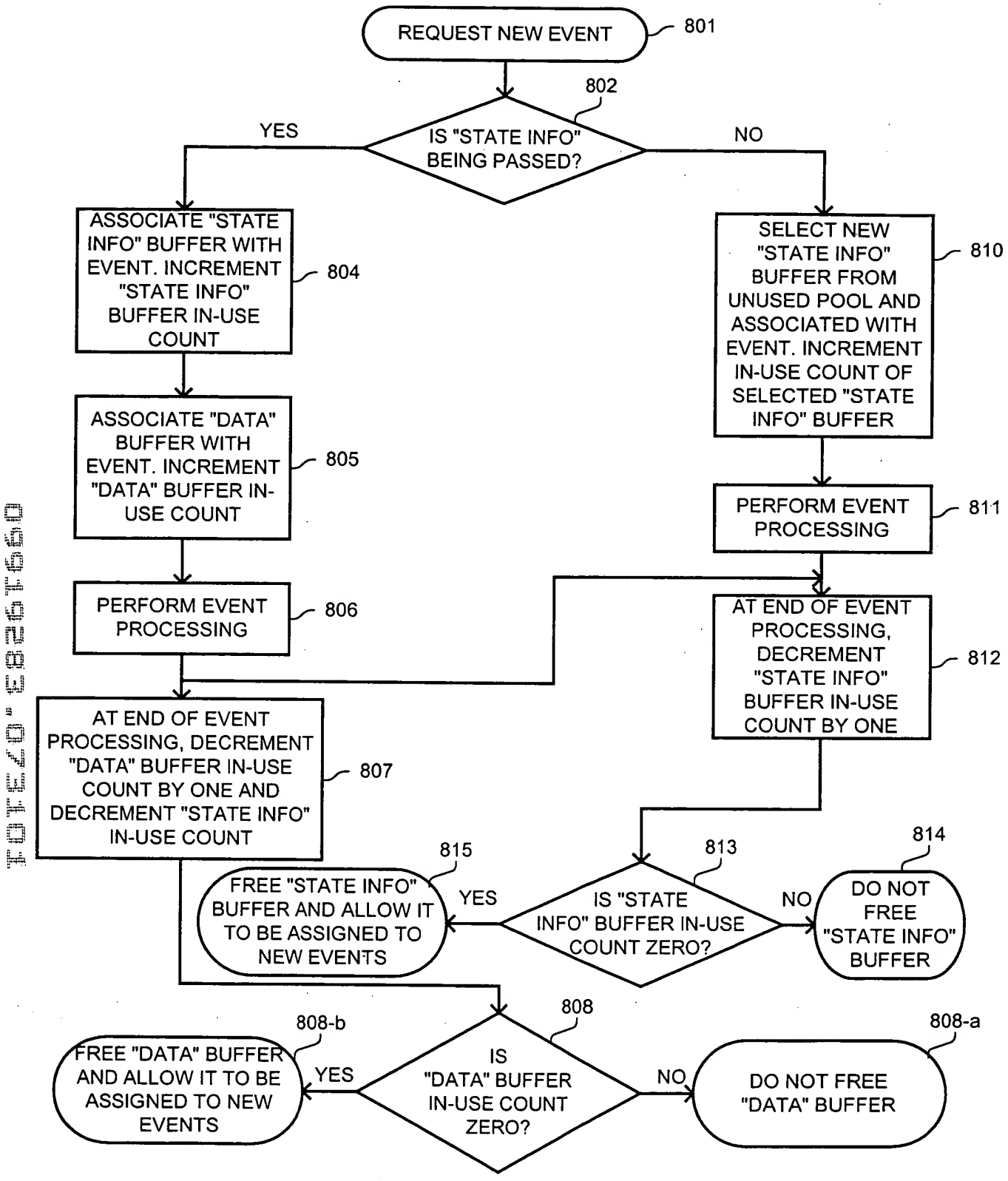

REQUEST NEW EVENT
801
802
IS "STATE INFO" BEING PASSED?
YES
NO
ASSOCIATE "STATE INFO" BUFFER WITH EVENT. INCREMENT "STATE INFO" BUFFER IN-USE COUNT
804
ASSOCIATE "DATA" BUFFER WITH EVENT. INCREMENT "DATA" BUFFER IN-USE COUNT
805
PERFORM EVENT PROCESSING
806
AT END OF EVENT PROCESSING, DECREMENT "DATA" BUFFER IN-USE COUNT BY ONE AND DECREMENT "STATE INFO" IN-USE COUNT
807
SELECT NEW "STATE INFO" BUFFER FROM UNUSED POOL AND ASSOCIATED WITH EVENT. INCREMENT IN-USE COUNT OF SELECTED "STATE INFO" BUFFER
810
PERFORM EVENT PROCESSING
811
AT END OF EVENT PROCESSING, DECREMENT "STATE INFO" BUFFER IN-USE COUNT BY ONE
812
813
IS "STATE INFO" BUFFER IN-USE COUNT ZERO?
YES
NO
815
FREE "STATE INFO" BUFFER AND ALLOW IT TO BE ASSIGNED TO NEW EVENTS
814
DO NOT FREE "STATE INFO" BUFFER
808
IS "DATA" BUFFER IN-USE COUNT ZERO?
YES
NO
808-b
FREE "DATA" BUFFER AND ALLOW IT TO BE ASSIGNED TO NEW EVENTS
808-a
DO NOT FREE "DATA" BUFFER

FIGURE 8

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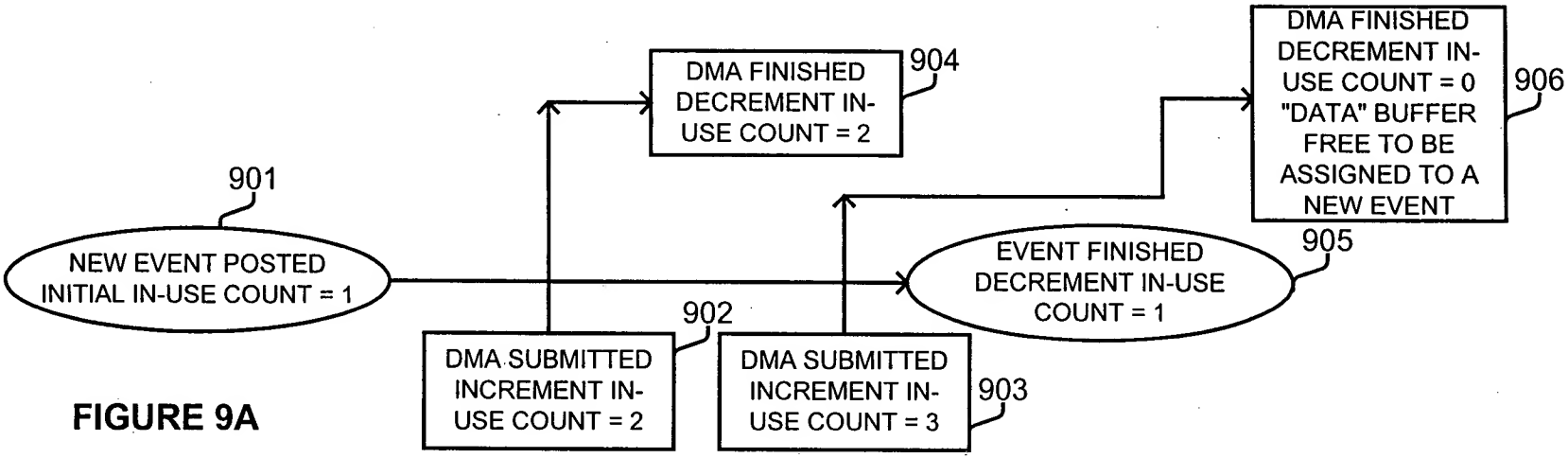

FIGURE 9A

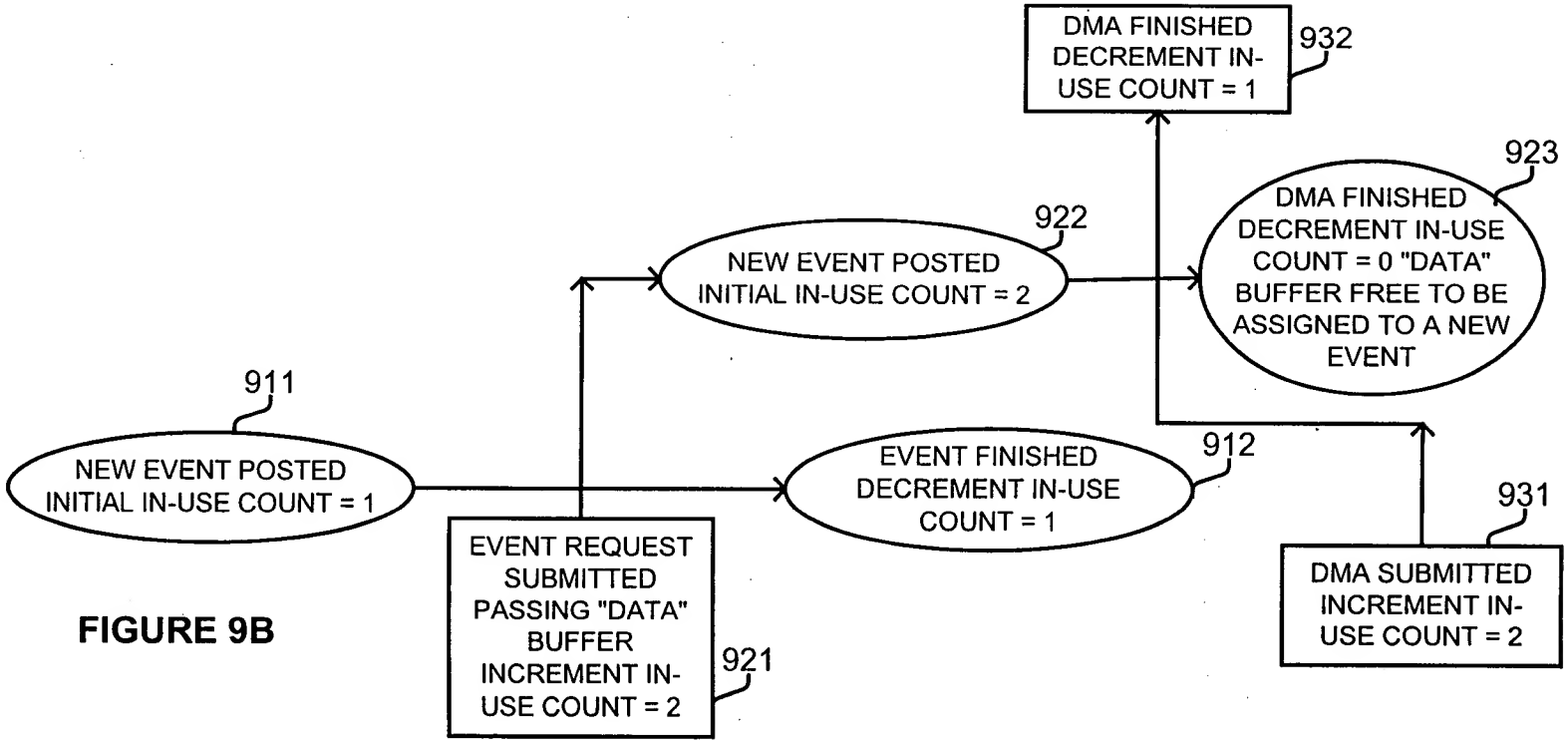

FIGURE 9B